Command Detector SNR Estimator and Lock Status Monitor Circuitry

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A breadboard of the command detector signal-to-noise-ratio estimator and lock status monitor was built on a wire-wrap card. The breadboard was integrated with the Standard Command Detector, and its performance was measured. The design, design constraints, and construction of the breadboard are described. The performance is shown to agree with the theoretical model

I. Introduction

The command detector signal-to-noise-ratio estimator and lock status monitor (SNORE–LOCK) was developed from work centering around data-aided tracking receivers (Ref. 1). The advantage of this approach is that it is insensitive to the magnitude of the input signal. This is particularly important in connection with the multiple rate command detector activity (Ref. 2).

The SNORE–LOCK circuit was designed to interface with, and become a part of, the Standard Command Detector being developed for the NASA Low Cost Systems Office. The circuit accepts values from the matched filters of the command detector and calculates a signal-to-noise-ratio (SNR) estimate (SNORE). Using several values of this estimate, it decides the lock status of the detector.

II. Theory of Operation

The design of the SNORE–LOCK circuit will be described below starting at the functional level and progressing to the logic level. A description as if it were a computer program is presented to clarify the sequencing of events within the circuit.

A. Functional Description

A functional block diagram of the SNORE–LOCK circuit is shown in Fig. 1. The diagram illustrates the data flow and functional processing within the circuit.

Starting at the left of the diagram, N values of each of two data types are accumulated in magnitude. The value of DATA represents an inphase correlation when the detector is locked. Likewise the value of ERROR represents the quadrature phase correlation. The inphase value is a measure of the signal, while the quadrature phase value is a measure of the noise.

A ratio of the accumulated values is then computed. This computed value is called SNORE. SNORE values are both accumulated for telemetry use and compared with a fixed digital threshold for lock detection. K successive comparisons are used in the lock indication algorithm.

In the breadboard version of the circuit, the values of N,K and the threshold are digitally selectable. In the flight unit these values would be fixed at manufacture.

B. Logical Description

The logic block diagrams of Figs. 2 and 3 expand upon the above functional description of the previous section. All arithmetic operations within the processor are bit-serially performed.

Values of DATA and ERROR received from the detector are scaled to fit within the accumulator registers of the processor. Since a resolution of 0.25 in SNORE is required, the value of ERROR is divided by 4 before it is accumulated. This permits the use of an integer division algorithm.

At the correct time, the values in the scaling registers are transferred through conditional complementors (C/C) and accumulated. The multiplexor at the input of each accumulator selects the source of information depending upon the phase of processor operation.

During the accumulation phase, the C/C outputs are the sources for the accumulators. During the division or "compute" phase, the value of the divisor is added to the dividend. Since ERROR was accumulated as a negative absolute value, this results in a subtraction. For each successful subtraction (that is, where the result is still greater than zero), the quotient is incremented. This incrementing is accomplished with the adder previously used to obtain the divisor. The sharing of this adder reduces the package count and power requirements at a small cost in complexity—the addition of a multiplexor.

The timing logic provides the signals and clocks used to control operations within the processor. After N accumulations are performed, the division process is started. Should the detector present new values of DATA and ERROR before the division is complete, the operation reverts back to the accumulation phase. This limits the maximum value of SNORE at high symbol rates (above 500 symbols/s). This does not affect the lock indicator operation as the maximum is about twice the nominal value for threshold lock indication.

The value of SNORE is used by the lock indicator (Fig. 3), and is accumulated for presentation to the telemetry subsystem.

The quotient or SNORE value is compared with a fixed digital threshold. K successive values that are greater set the detector lock indicator, while K successive values that are not greater reset the lock indicator. When set, the lock indicator indicates in-lock. K successive decisions which are not members of these two groups cause no change in lock indication.

C. SNORE–LOCK Algorithm

The SNORE calculation is performed in two steps or phases. During the first phase, a number of samples of the DATA and ERROR register values from the detector are accumulated. During the second phase, the accumulated results are used to obtain a ratio which is a measure of the SNR. In addition to these two active phases, there is a quiescent phase in which no processing is performed.

In order to place the relationships in a logical order, the following discussion will treat the SNORE–LOCK processing as a computer program. The flow chart of Fig. 4 would represent the actual processing if each action could be accomplished in "no" time. Since the processing action requires a finite amount of time, some elements in the hardware implementation have been included to provide for "multiprocessor" capability. Each element of the flowchart, identified by number, is presented below.

Block 1 illustrates a waiting function. Waiting is necessary to synchronize data transfers between the detector and the SNORE processor. The detector has data ready for transfer 32,000 times a second. The only data transfer that is used by the SNORE processor occurs at the end of a symbol time. (Here "symbol" represents one unit of information in the command message. The term "symbol rate" will be used for command bit rate to prevent confusion.) Each data transfer is saved except the one at the beginning of the symbol period (see Blocks 2 and 3). By this method the values of the DATA and ERROR registers in the detector at the end of a symbol period are available for use at the correct time.

Block 4 tests the "First Sum Flag." If successful, it indicates that a value of SNORE is available and must be processed. The processing is added to the loop once for every N accumulations (see Block 18). In Block 5 this flag is reset, the "SNORE counter" is incremented, and, if the counter value equals 16 (Block 6), the value in the "SNORE accumulator" is made available to the telemetry subsystem. At the same time both the counter and accumulator are cleared (Block 7). In Block 8 the new value of SNORE, indicated by the flag, is accumulated.

Block 9 represents the lock detector test of SNORE against the fixed threshold. If the value is not greater than the threshold, "Flag" is set (set = 1) (see Blocks 10 and 11). The lock indicator is reset if the last K "Flags" were one. This is shown in Blocks 12 through 15. The value of the latest "Flag" is added to storage and the $(K + 1)$st value is dropped (Block 16). After this is complete, the flow returns to the main loop.

The values saved by the operations of Block 3 are summed, in absolute value, in the dividend and divisor registers. The "symbol counter" is also incremented (Block 17). If this count has not reached the present value N (Block 18), processing is returned to the wait loop at Block 1. If it has reached N, "First Sum Flag" is set (Block 19) and the quotient register is cleared (Block 20).

The value of SNORE is computed by an integer division algorithm. This algorithm is illustrated in Blocks 21, 22, and 23. The value in the dividend register, representing an accumulation of ERROR values, is repeatedly subtracted from the value in the divisor register. The results of each subtraction are returned to the divisor register. If this result is greater than zero, the quotient is incremented; if not, the processing is completed and the flow is returned to Block 1.

Two other conditions will stop the division process. If the quotient will overflow on the next successful cycle (Block 24) or if time has run out—indicated by the signal "Last Sample" (Block 25)—division is stopped and the flow returned to the wait loop at Block 1.

III. Description of Hardware

The breadboard SNORE–LOCK circuit was designed to provide a test vehicle for the algorithm and to approach, as closely as possible, the flight qualifiable form of the circuit. These are somewhat contradictory constraints.

The following paragraphs will expand upon the constraints and illustrate, briefly, the resulting equipment.

A. Implementation Constraints

In order to minimize the flight qualification development phase of the Standard Command Detector, including the SNORE–LOCK circuit, the design of the breadboard was constrained to use those circuit elements which had already passed Preferred Part Qualification. The second most important consideration was that of power dissipation. Therefore, 54L series logic elements were used, except where speed considerations prevented their use. Finally, package count, a measure of complexity, was used to constrain the design.

The breadboard design included parameter entry logic which would not be used in the flight design. This was done to facilitate the optimization of those parameters.

B. Construction

The breadboard was built on a wire-wrap card (type B). A photograph of the completed breadboard is presented as Figs. 5 and 6. This approach was used because of extensive experience with it for both breadboard and finished systems. In addition, the "Card" is supported by mounting and interconnect hardware and support software to permit rapid and accurate construction and documentation. Further, the wire-wrap approach facilitates changes while maintaining stable "brass board" quality.

IV. Integration and Preliminary Performance Tests

The design, construction, and functional testing of the SNORE–LOCK was performed independently of that performed for the command detector. The interface between the two sections was the only aspect of the total system design that required mutual and coordinated effort.

A. Integration

The integration of the SNORE–LOCK was accomplished in an orderly manner with no difficulties. Certain signals of the system were inspected after integration to validate that the interface had been done properly.

B. Preliminary Performance Tests

Preliminary performance tests of the SNORE–LOCK circuit were performed using the command detector, a simulated signal channel, and specialized instrumentation. Two types of tests were conducted: (1) the value of computed SNORE was compared with that of the input SNR, and (2) the probability of falsely indicating the lock status at an input of 10.5 dB SNR.

1. SNORE Value Tests. The value of SNORE was measured as a function of bit rate and input SNR. At the time of the tests the detector loss had been measured to be 1.5 dB. Figure 7 presents the results of these tests. Ten values of DATA and ERROR were accumulated for each SNORE computation. The 8-bit per second results are thought to be caused by truncation errors. This has not been modeled as yet (Ref. 3).

2. Lock Indicator Tests. The performance of the lock indicator was measured at one bit rate and one input signal level. Ten accumulations of DATA and ERROR and two successive comparisons were used for the lock indication (See Fig. 8). In addition, the bit error rate (BER) at the output was measured. This allowed a closer comparison of the results with the theoretical model (Ref. 4).

From these results it would appear that the false-in-lock (FIL) probability is better than that predicted by theory. Unfortunately, this results from a design decision which resulted from truncation problems. The error accumulation is set to −1 at the start of an accumulation cycle to prevent dividing by zero. This lowers the values of SNORE and results in shifting the lock probabilities curves to the left. At low values of threshold, truncation errors affect the P_{FIL} result.

V. Conclusions

The results of the preliminary tests indicate that the operation of the SNORE and lock circuits is as predicted by the theory. Extensive and expensive discrete simulations would be required to improve upon these results.

References

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2. Emerson, R. F., "A Multiple-Rate Command System," in *The Deep Space Network Progress Report 42-25*, pp. 94–107, Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1975.
3. Lipes, R. G., "Analysis of Command Detector Signal-to-noise Ratio Estimator," in *The Deep Space Network Progress Report 42-31*, pp. 75–83, Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1976.
4. Lipes, R. G., "Analysis of Command Detector In-Lock Monitoring," in *The Deep Space Network Progress Report 42-32*, pp. 70–73, Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1976.

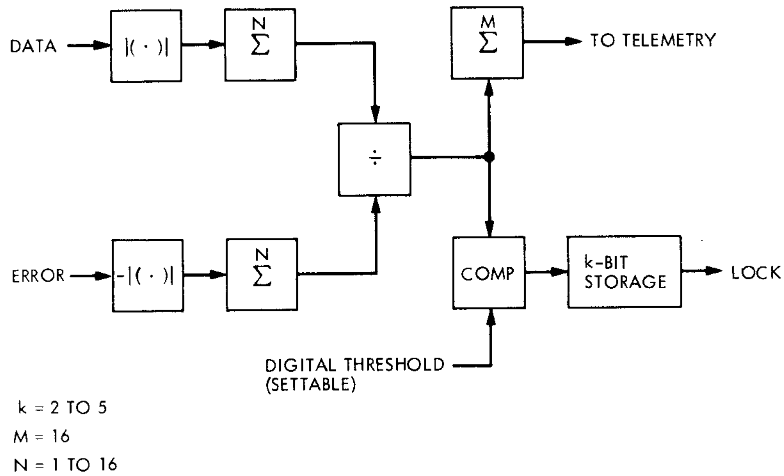

Fig. 1. Functional block diagram of SNORE–LOCK

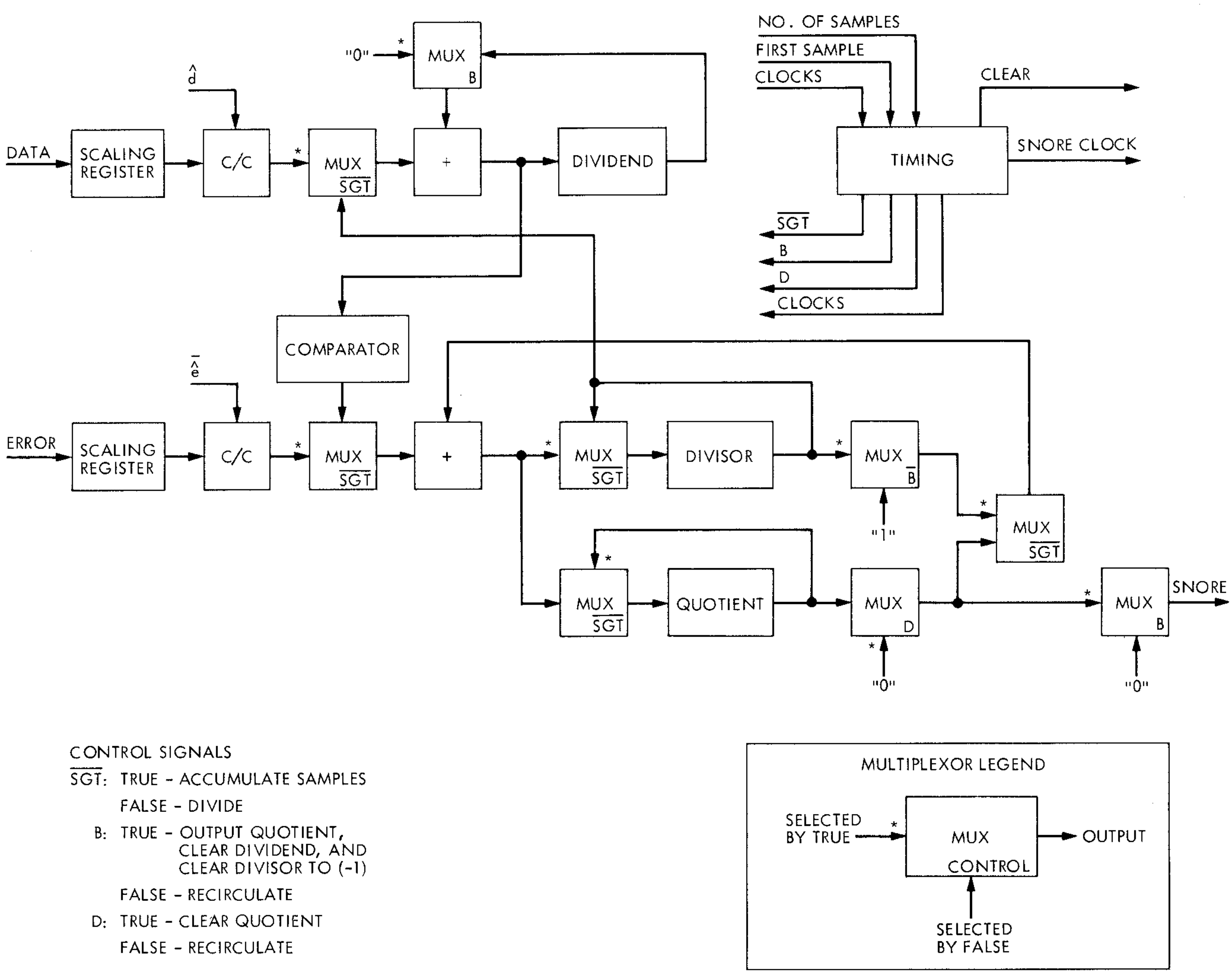

Fig. 2. Logic block diagram of accumulators and divider

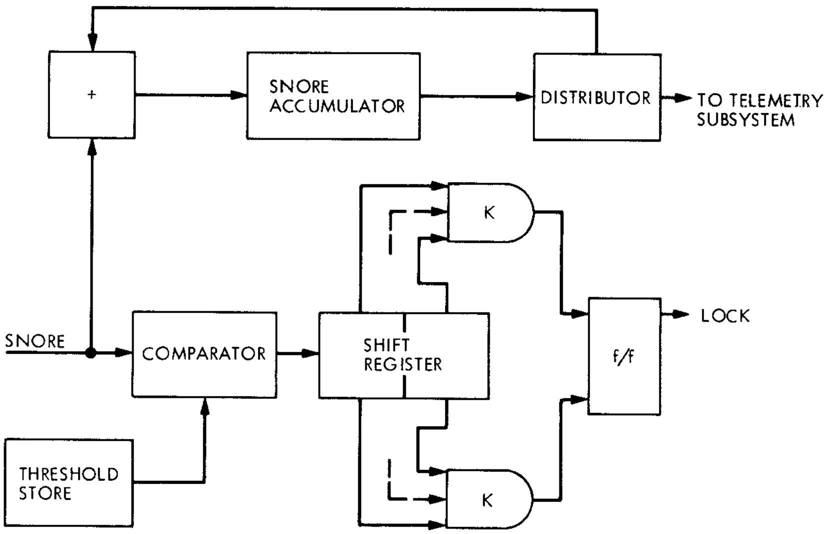

Fig. 3. Logic block diagram of SNORE accumulator and LOCK indicator

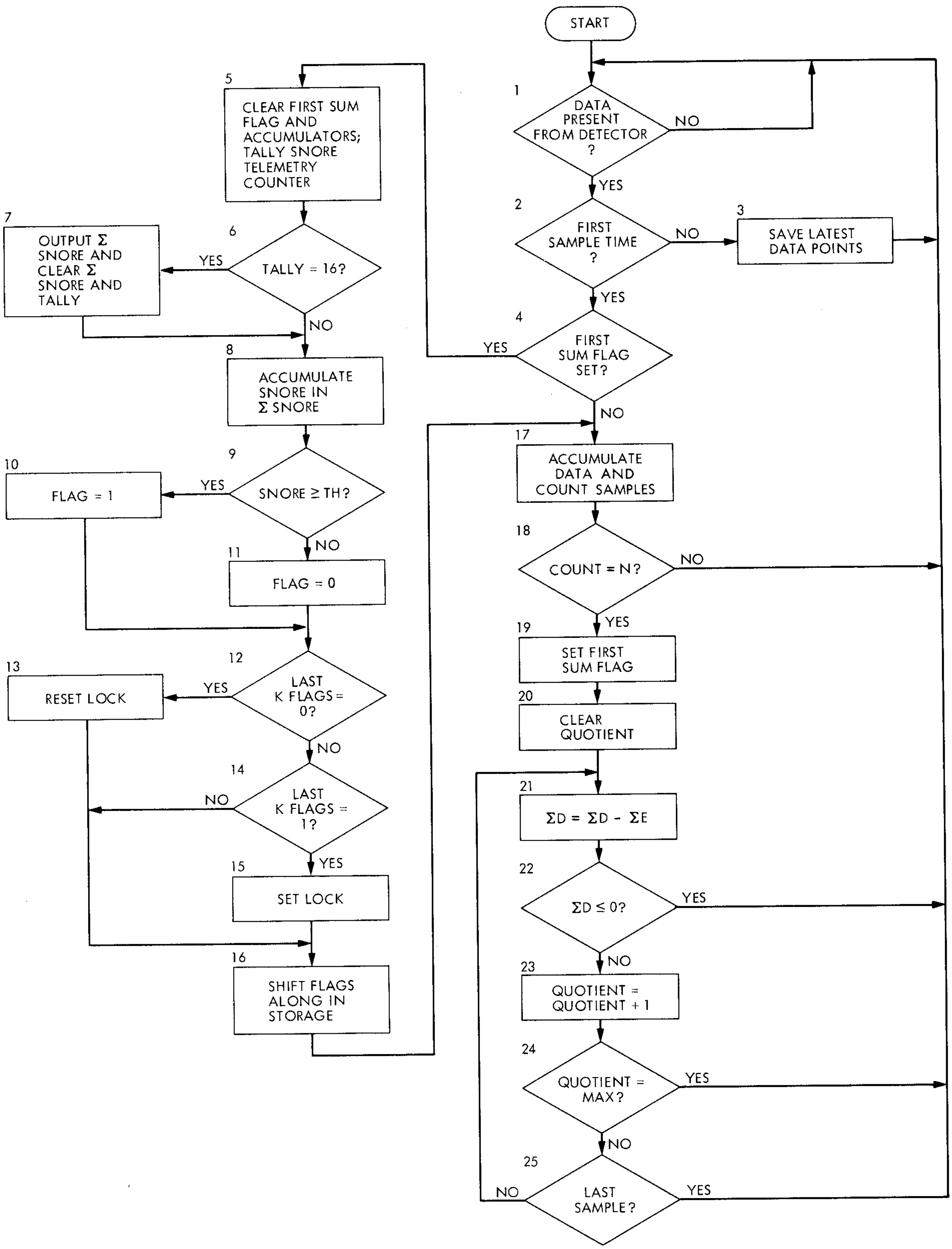

Fig. 4. SNORE–LOCK algorithm flowchart

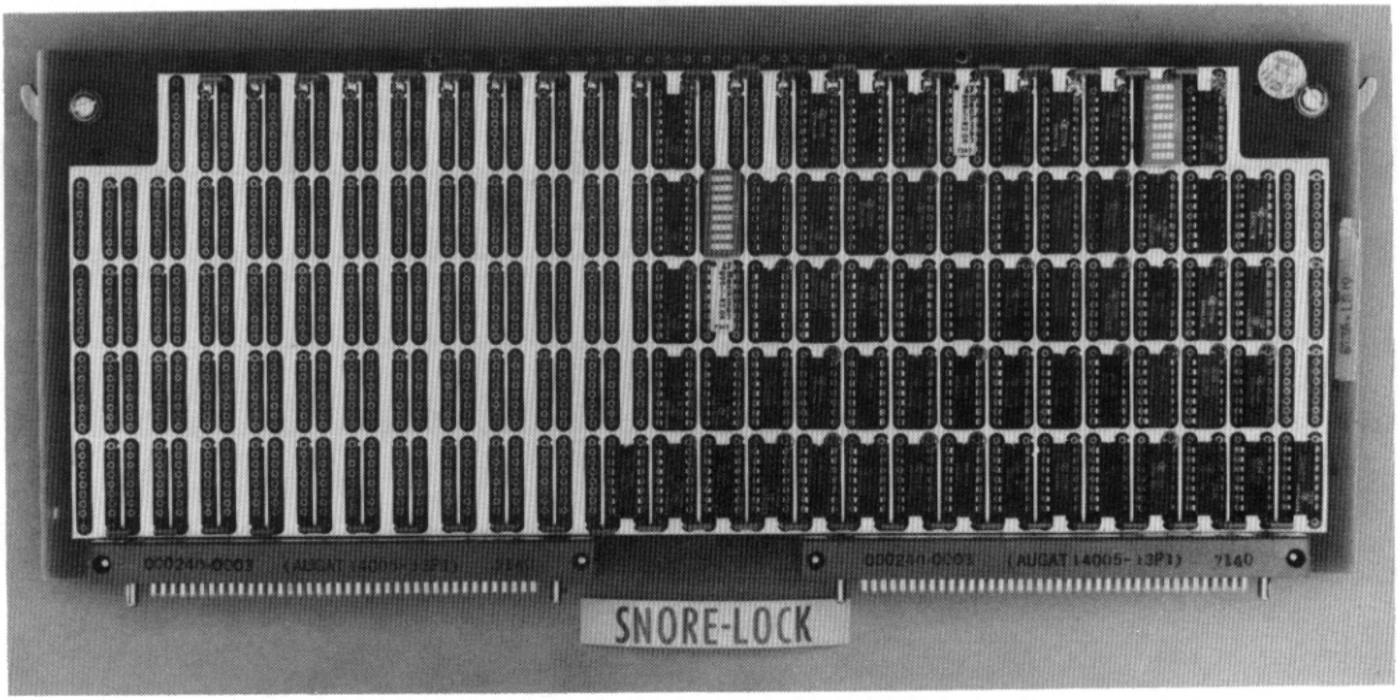

Fig. 5. Component side of SNORE-LOCK wire-wrap card

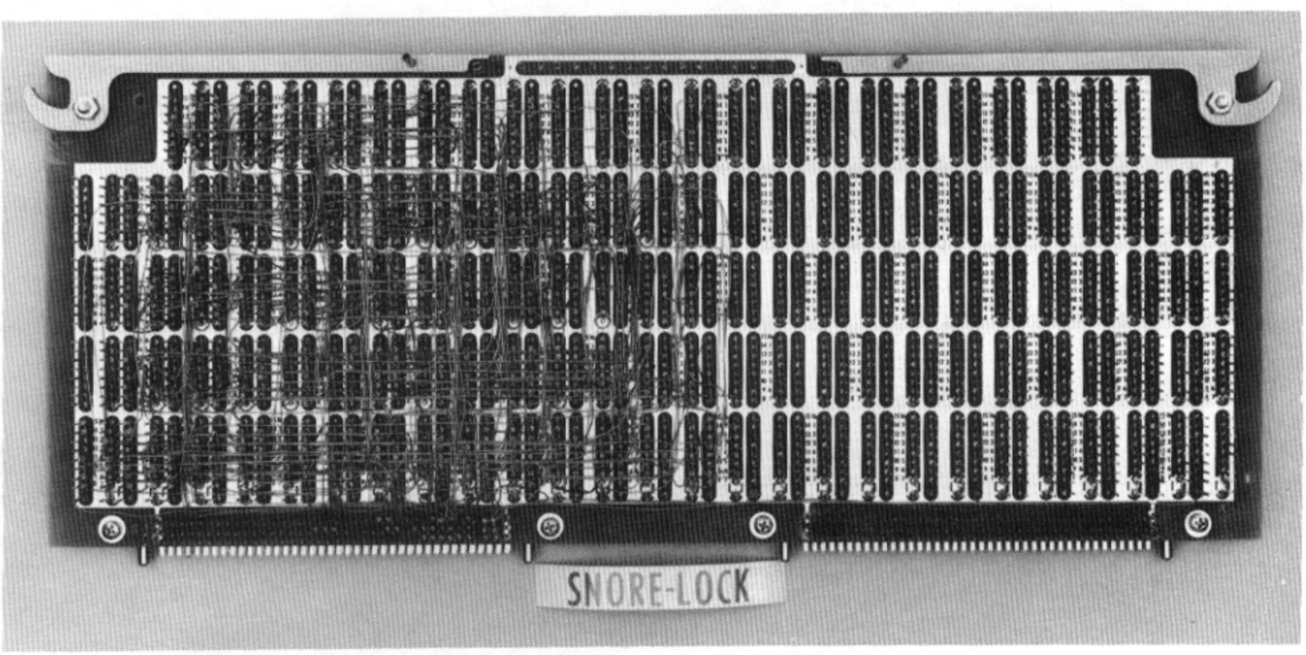

Fig. 6. Wiring side of SNORE-LOCK wire-wrap card

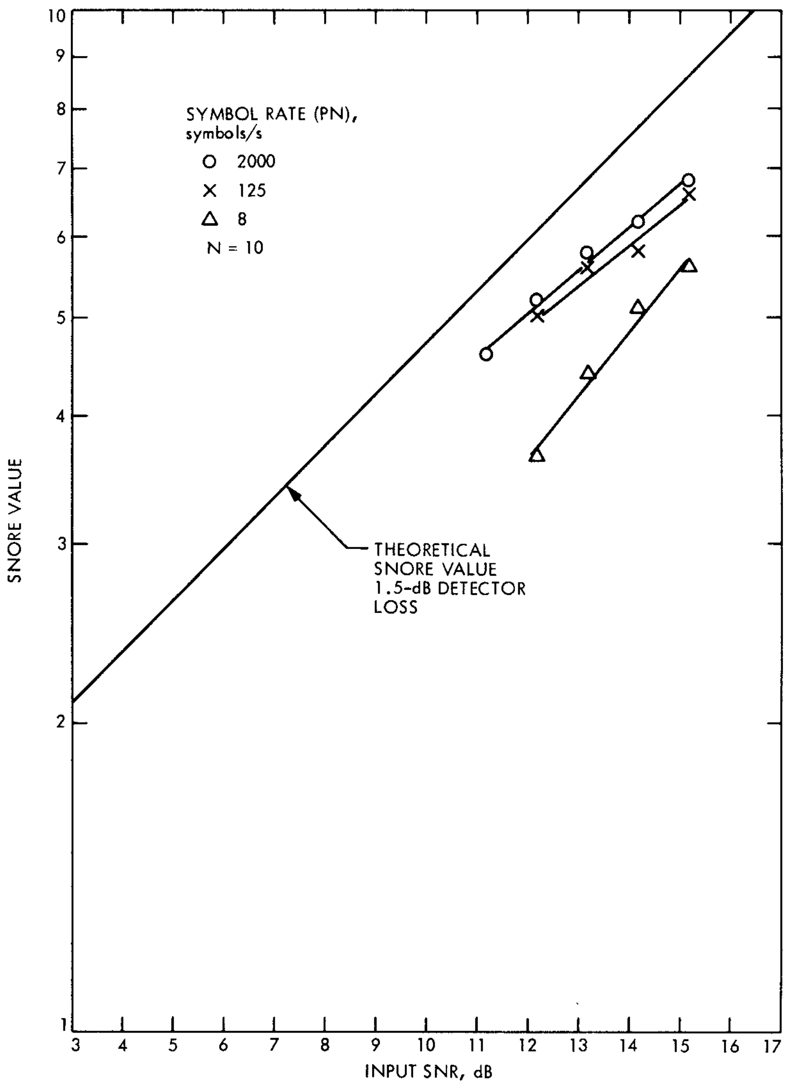

Fig. 7. Input SNR vs SNORE at several symbol rates

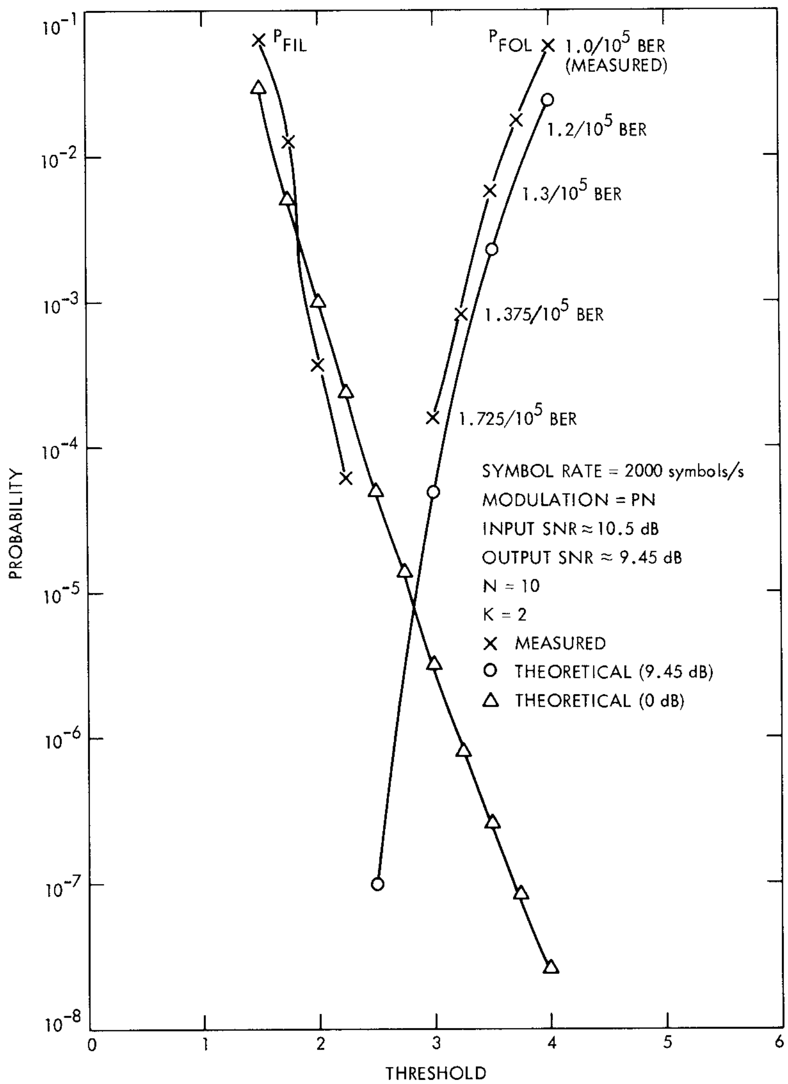

Fig. 8. LOCK indicator tests